A1 cndd.

linear media. This phenomenon is not effectively addressed by traditional linear equalization techniques due to the non-casual nature of the impairment. A method is presented to reduce the effects of pulse spreading on hard-decision error rate in communication systems affected by this problem. The method utilizes multiple decision thresholds for each data bit. Post-processing of the multiple decision data is employed to reduce the data to a single hard decision per bit. The multiple data thresholds are adjusted for optimal mitigation of the spreading effect.

On page ~~6,~~ beginning at line 13 and continuing to line 24, please delete the paragraph beginning "Fig. 3...", and replace it with the following paragraph:

A2

Fig. 3 is a schematic block diagram of the present invention non-casual channel equalization communication system. The system 100 comprises a multi-threshold decision circuit 102 having an input on line 104 to accept a non-return to zero (NRZ) data stream, and an input on line 106 to accept threshold values. The multi-threshold decision circuit 102 has outputs on line 108 to provide bit estimates responsive to a plurality of voltage threshold levels. A non-casual circuit 110 has inputs on line 108 to accept the bit estimates from the multi-threshold decision circuit 102. The non-casual circuit 110 compares a current bit estimate (a first bit) to bit values decisions made across a plurality of clock cycles. The non-casual circuit 110 has an output to supply a bit value decision for the current bit estimate determined in response to the non-casual bit value comparisons.

Specification was replaced in amendment B of 7/1/2008 D-2

On page 6, beginning at line 25 and continuing to page 7, line 14, please delete the paragraph beginning "The causal circuit...", and replace it with the following paragraph:

A3

The non-casual circuit 110 includes a present decision circuit 112, a future decision circuit 114, and a past decision circuit 116. The future decision circuit has inputs connected to the mutli-threshold circuit outputs on line 108. The future decision circuit 114 has outputs to supply the first bit estimate and the third bit value (as explained below). The present decision circuit 112 has inputs to accept the first bit estimate, the third bit value, and a second bit value from the past decision circuit 116. The present decision circuit 112 compares the first bit estimate in the data stream to the second bit value received prior to the first bit estimate, represented as being supplied from the past decision circuit 116 on line 118. The present decision circuit 112 also compares the first bit estimate to the third bit value received subsequent to the first bit estimate, represented as being from the future decision circuit 114 on line 120. The present decision circuit 112 has an output on line 122 to supply a first bit value determined in response to comparing the first bit estimates to the second and third bit values.

On page 8, beginning at line 9 and continuing to line 18, please delete the paragraph beginning "In some aspects...", and replace it with the following paragraph:

A4 Cm't

In some aspects of the system, the multi-threshold circuit 102 accepts an NRZ data stream encoded with forward error correction

specification was replaced in amendment B of 7/1/2008 [illegible]

(FEC). Then, the system 100 further comprises a forward error correction (FEC) circuit 130 having an input on line 122 to receive the (first) bit values from the non-casual circuit 110. The FEC circuit 130 decodes the incoming data stream and corrects bit value in response to the decoding. The FEC circuit 130 has an output on line 106, specifically lines 106a, 106b, and 106c, to supply threshold values to the multi-threshold circuit 102 in response to the FEC corrections. The FEC circuit 130 has an output on line 132 to supply a stream of corrected data bits.

A4 cncld.

On page 13, beginning at line 1 and continuing to line 14, please delete the paragraph beginning "In some aspects...", and replace it with the following paragraph:

A5

In another aspect of the system 600, the third threshold generator accepts the NRZ data stream input, shown as a dotted line 104. The third threshold generator 606 maintains the average voltage, or a digital representation of the average voltage, on the NRZ data stream input. Note, this is a measurement of the NRZ data stream without regard to non-casual analysis, or the analysis of bit values. The third threshold generator 606 supplies the third threshold (Vopt) at an output on line 106c in response to the measured average. The third threshold can be set to the measured average, for example. Note in this aspect, the input lines 106a and 106b are not needed. With pseudorandom scrambling it assumed that the average voltage is a result of an equal number of "0" and "1" bits being received on line 104. This method of generating the third threshold is very effective when the noise distribution is symmetrical.

specification was replaced in Amendment B filed 7/1/2002